2. Low-Noise Step-Down Switched-Capacitor Converter

- Design a step-down converter based on the LTC3251 integrated circuit using the circuit topology shown in Figure 2.1, with the specifications summarized in Table 1. the component values obtained in your design with those given in Figure 2.1.
- Run simulations using LTSPICE to verify the design.

  Continuous mode operation with spread spectrum

  Output voltage using Ro = $1\,K\Omega$

  Output voltage using Ro = $3.3\,K\Omega$

  Transient response to a load step

  Line regulation

  Load regulation

  Burst mode with spread spectrum

  Output voltage using Ro = $47\,\Omega$

  Transient response to a load step

  Line regulation

  Load regulation

  Super-burst mode operation

  Output voltage using Ro = $47\,\Omega$

  Transient response to a load step

  Line regulation

  Load regulation

  Shortcircuit protection

  Noise
- Build a prototype using the provided gerber file and part list.
- Obtain the following experimental results

  Continuous mode operation with spread spectrum

  Output voltage using Ro = $1\,K\Omega$

  Output voltage using Ro = $3.3\,K\Omega$

  Transient response to a load step

  Line regulation

  Load regulation

  Burst mode with spread spectrum

  Output voltage using Ro = $47\,\Omega$

  Transient response to a load step

  Line regulation

  Load regulation

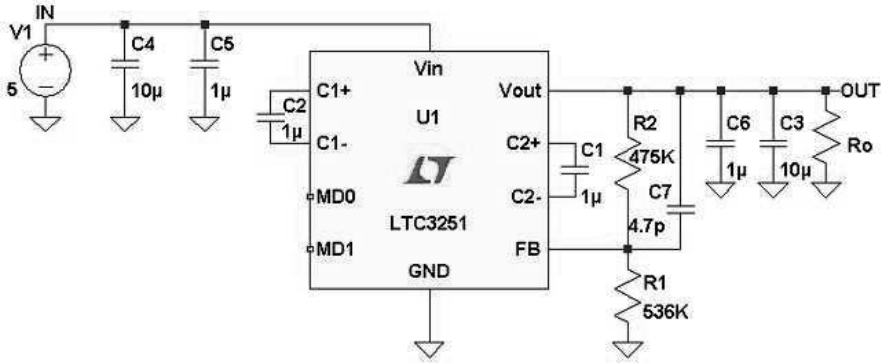

Figure 2.1: Schematic diagram of the low-noise switched-capacitor step-down converter.

Table 1: Design specifications.

Parameter	Minimum	Typical	Maximum	Unit
Vin	3.5	5	5.5	V
Vout	1.44	1.5	1.56	V
output voltage ripple in continuous mode			3	mVpp
output voltage ripple in burst mode			10	mVpp
output voltage ripple in super burst mode			45	mVpp
Iout in continuous mode and burst mode			500	mA
Iout in super burst mode			40	mA
MD0, MD1 Low		GND		
MD0, MD1 Hi		Vin		
Efficiency		$\frac{Pout}{Pin}$		

Super-burst mode operation

Output voltage using Ro = 47Ω

Transient response to a load step

Line regulation

Load regulation

Shortcircuit protection

Noise

Efficiency

The student should read first the data sheets of the LTC3251 IC before proceeding.

2.1. LTC3251

The LTC3251 is a dual-phase switched-capacitor converter. Figure 2.2 shows its pin assignment.

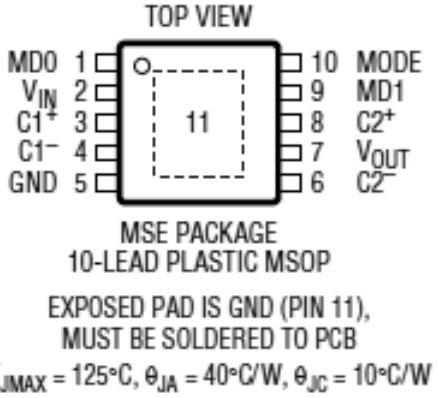

Figure 2.2: Pin assignment of the LTC3251. (Reprinted with permission of Linear Technology Corporation)

Table 2: Operating modes.

MD1	MD0	Operating mode
0	0	Suspended
0	1	Spread spectrum with burst
1	0	Spread spectrum continuous mode
1	1	Super burst

Pin function

MD0 (Pin 1) / MD1 (Pin 9) define the operating mode, according to Table 2.

MD0 and MD1 are high-impedance CMOS inputs and should not be left unconnected.

- Vin (Pin 2): input DC voltage supply.
- $C1^+$(Pin 3) and $C1^-$(Pin 4): Positive and negative terminals of one of the external switched capacitors.
- $C2^+$(Pin 8) and $C2^-$(Pin 6): Positive and negative terminals of one of the external switched capacitors.
- GND (Pin 5, 11): Ground.
- Vout (Pin 7): Regulated output voltage.
- MODE (Pin 10): Feedback input. A resistive voltage divider should be connected to Vout. A low voltage sets the spread spectrum mode. A high voltage disables the spread spectrum mode and sets the maximum switching frequency.

Operation

Figure 2.3 shows a simplified functionl diagram of the LTC3251.

The output voltage is sensed by the external voltage divider (R1 and R2), the obtained signal is fed back to the error amplifier to regulate the load current. A two-phase clock is used to drive

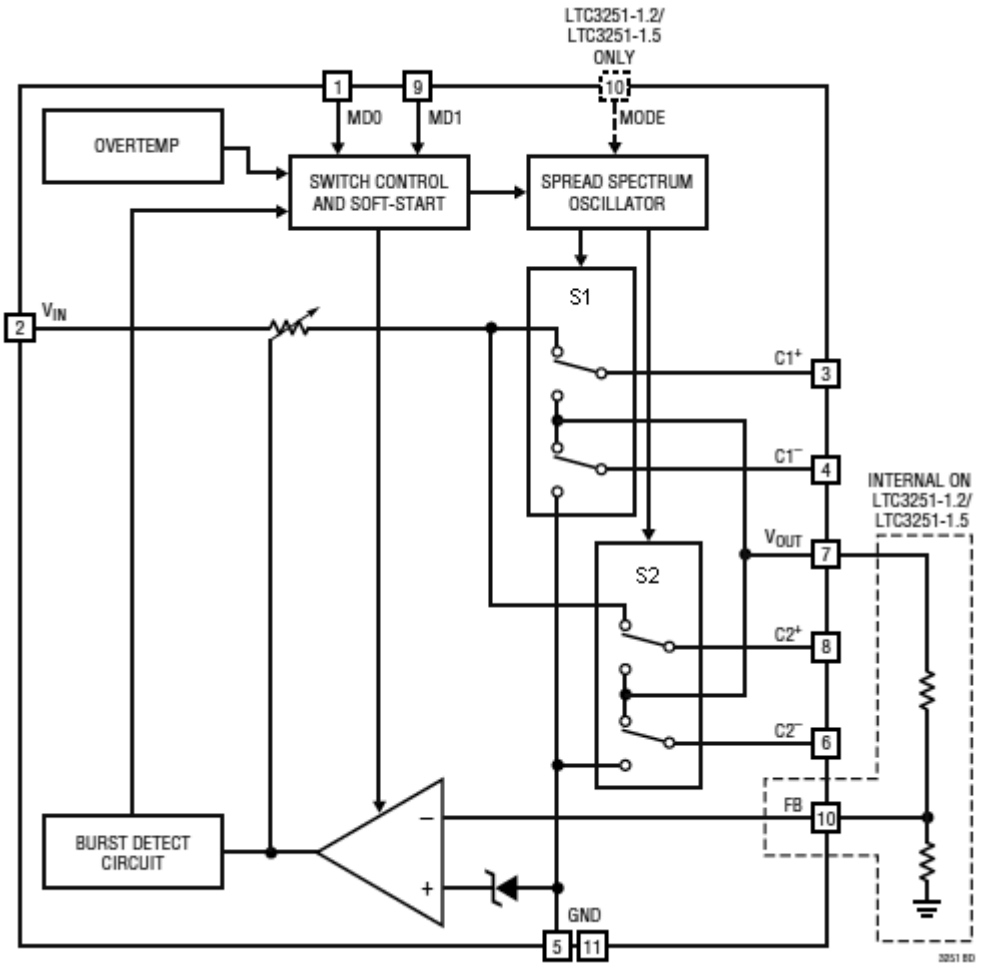

Figure 2.3: Simplified functionl diagram of the LTC3251. (Reprinted with permission of Linear Technology Corporation)

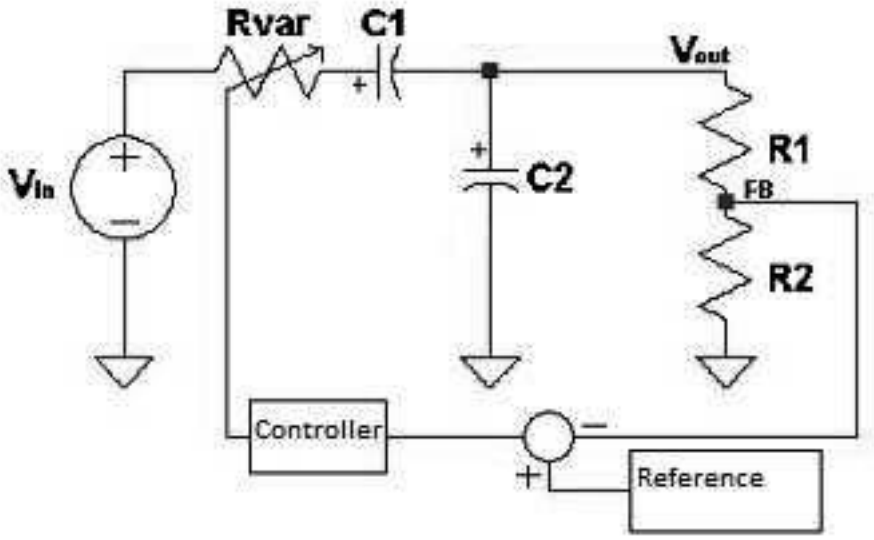

Figure 2.4: Equivalent circuit during the first clock phase.

the switches complementarily to charge the external capacitors. Figures 2.4 and 2.5 show the equivalent circuits during the first and second clock phases, respectively.

2.2. Component selection

Refer to Figure 2.1.

Output capacitor (C3)

The LTC3251 significantly reduces the output noise, but not completely. C3 is used to reduce the output voltage ripple. The ESR of C3 greatly impacts on the output noise and ripple. When both switches (S1 and S2) are open, all the output current flows through C3. Its current suddenly increases producing a voltage spike proportional to its ESR. Thus, a ceramic capacitor with low ESR ($\leq 0.08\Omega$) is normally chosen for C3.

C3 is also important from the stability point of view, since it holds the output voltage. Thus, C3 can be chosen to produce the dominant pole of the control loop. Refer to the LTC3251 data sheets for the selection of C3. Here a $10\,\mu F$ ceramic capacitor with ESR$\leq 0.08\Omega$ is selected. A $1\,\mu F$ ceramic capacitor (C6) is connected in paralell with C3 to improve the performance at high frequencies.

Input capacitor (C4)

Similarly to C3, C4 should have low ESR to attenuate the input voltage spike when both switches are open. When the output impedance of the input voltage source is relatively high, a load transient may cause a significative input transient that may be reflected at the output.The manufacturer reccomends choosing C4 $\geq 4.7\mu F$. We have chosen a $10\,\mu F$ ceramic capacitor for C4. Another $1\,\mu F$ ceramic capacitor (C5) is connected in parallel to improve the high frequency performance.

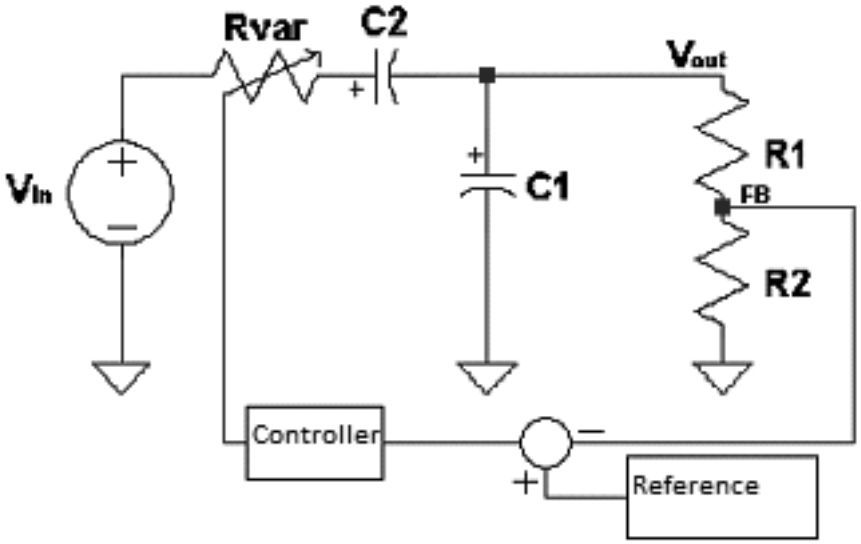

Figure 2.5: Equivalent circuit during the second clock phase.

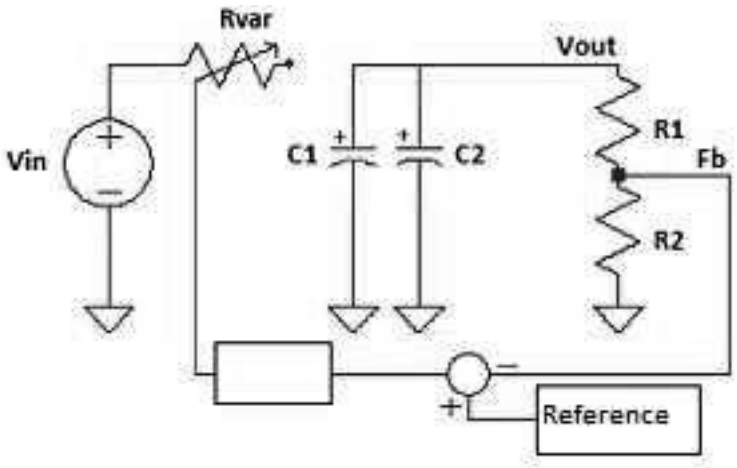

Figure 2.6: Equivalent circuit when both switches are open.

Switching capacitors (C1 and C2)

The manufacturer reccomends choosing C1 and C2 larger than $0.4\,\mu F$. We have used $1\,\mu F$ ceramic capacitors.

All capacitors use X5R or X7R materials for thermal and voltage stability.

Sensing resistors (R1 and R2)

The output voltage is programmed by the resistive voltage divider (R1-R2). The output voltage should be $1.5\,V$ the voltage at node Fb (Figure 2.1) should be $0.8\,V$. Thus,

$$VFb = Vout \cdot \frac{R1}{R1 + R2}, \tag{2.1}$$

regrouping,

$$\frac{R2}{R1} = \left(\frac{Vout}{VFb} - 1\right), \tag{2.2}$$

then

$$\frac{R2}{R1} = 0.875. \tag{2.3}$$

Choosing R1 = $536\,K\Omega$ yields R2 = $475\,K\Omega$.

These resistors create a pole in the control loop that is compensated by C7 ($4.7\,pF$).

2.3. Simulations

Linear Technologies® offers a SPICE-based simulator named LTSPICE that is freely available at www.linear.com. Simulation models for most of their products are available from this simulation program.

Continuous mode operation with spread spectrum

Figure 2.7 shows the schematic circuit used for simulation in continuous mode with spread spectrum.

Output voltage using Ro = 1KΩ . Figure 2.8 shows the output voltage at $1.5\,mA$. Figure 2.9 shows the output voltage ripple. Its peak to peak value is $10\,\mu V$.

Output voltage using Ro = 3.3Ω . Operating conditions close to the maximum loading (at $454\,mA$ close to $500\,mA$) are shown in Figure 2.10. Figure 2.11 shows the output voltage ripple. Its peak to peak value is $1.79\,mV$.

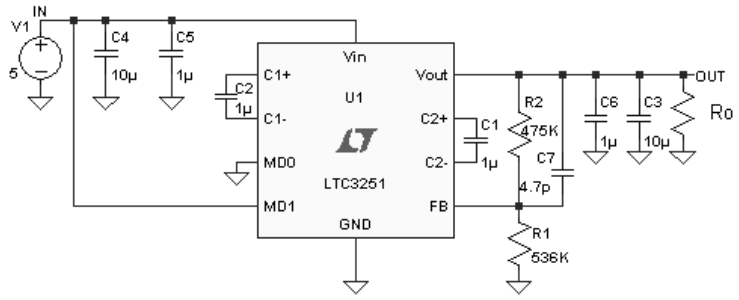

Figure 2.7: Schematic circuit used for simulation in continuous mode with spread spectrum.

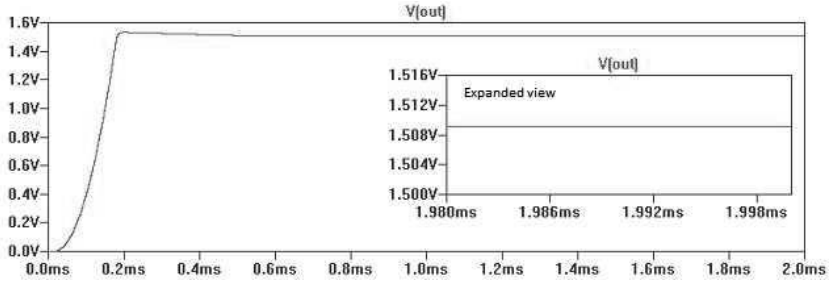

Figure 2.8: Output voltage at 1.5 mA.

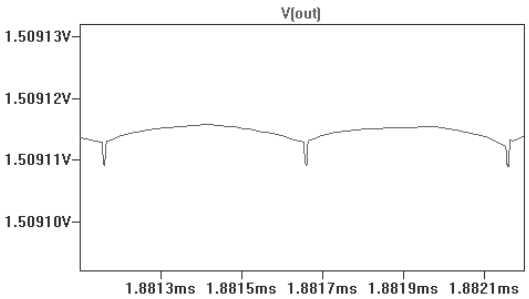

Figure 2.9: Magnified view of the output voltage to show the ripple.

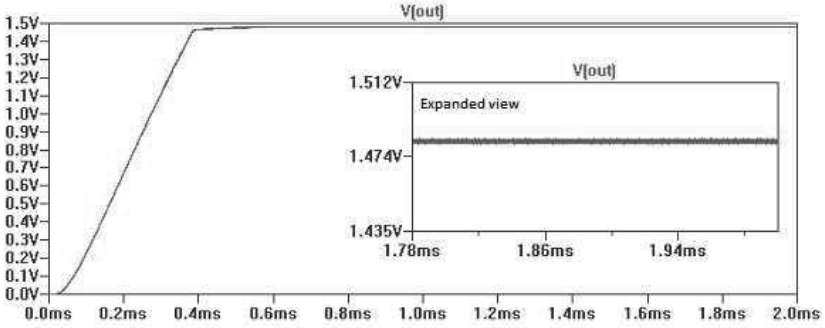

Figure 2.10: Output voltage at 454 mA.

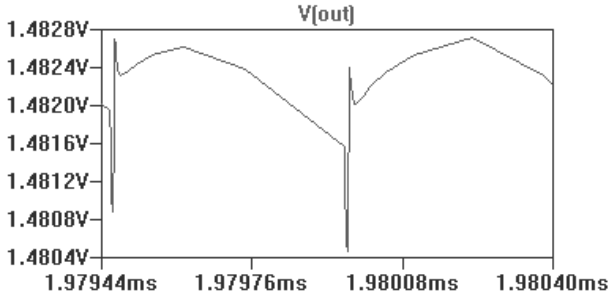

Figure 2.11: Magnified view of the output voltage to show the ripple.

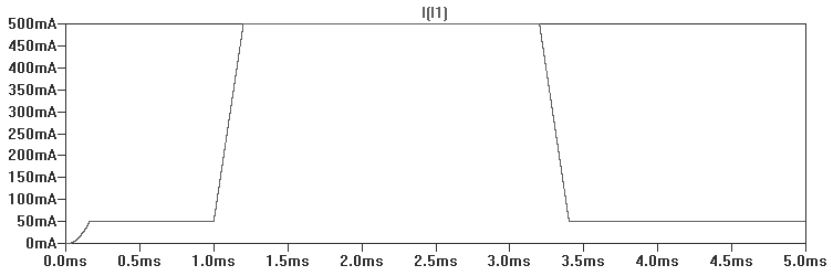

Figure 2.12: Load transient.

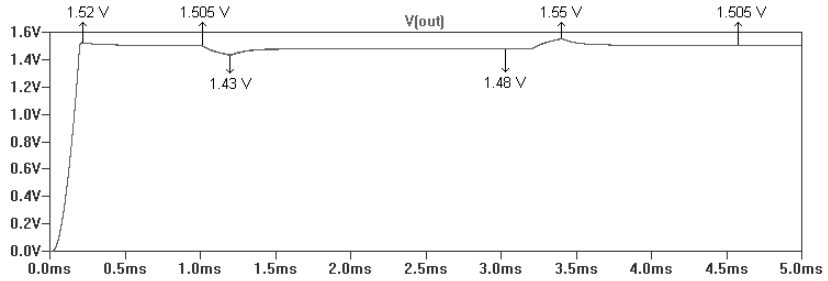

Figure 2.13: Transient response to the load transient.

Transient response to a load step. A load transient from 50 mA to 500 mA and back to 50 mA was simulated, as it is shown in Figure 2.12. The corresponding transient response is shown in Figure 2.13.

The clock signal for a 50 mA and 500 mA loads (without C3 and C6) are shown in Figure 2.14 and 2.15, respectively.

Figure 2.15 shows a random clock frequency.

Line regulation. Figure 2.16 shows the line regulation for three output currents.

Load regulation. Figure 2.17 shows the load regulation for Vin = 5 V.

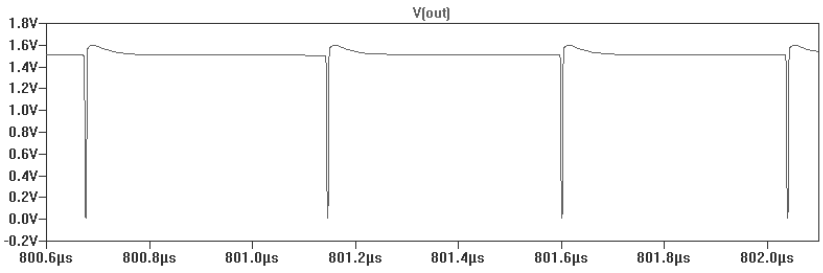

Figure 2.14: Clock signal at 50 mA.

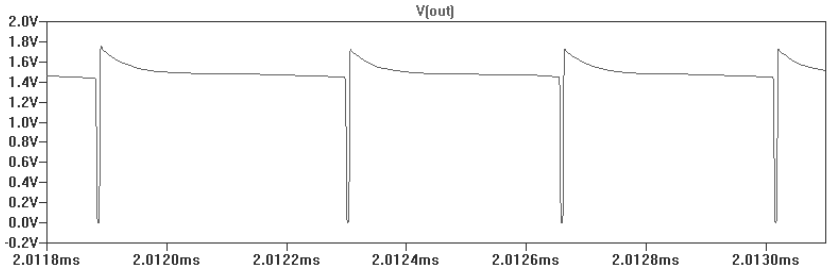

Figure 2.15: Clock signal at 500 mA.

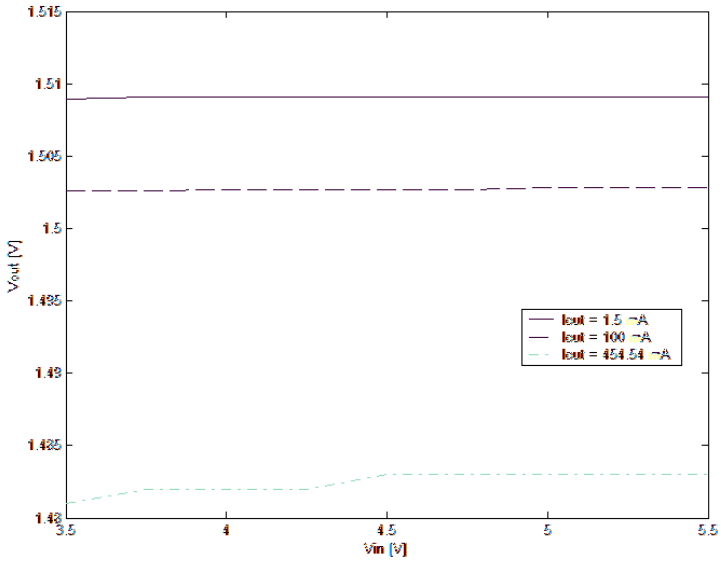

Figure 2.16: Line regulation in continuous mode.

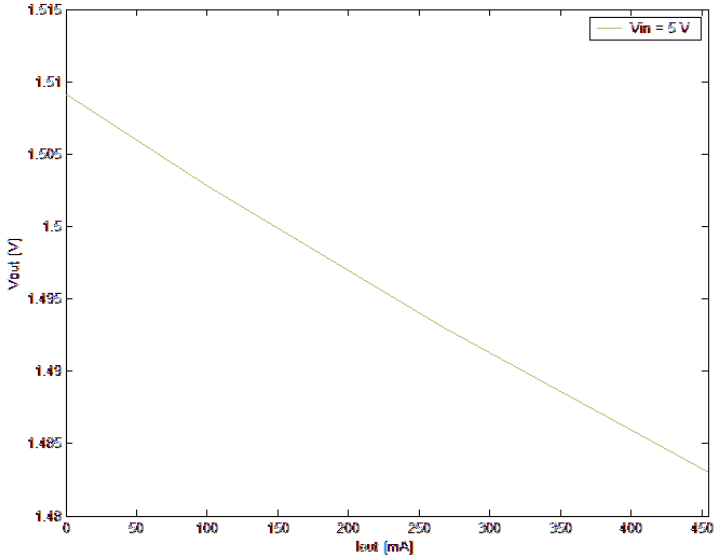

Figure 2.17: Load regulation in continuous mode.

Burst mode with spread spectrum

The schematic circuit used for the simulations in burst mode with spread spectrum is shown in Figure 2.18.

This operating mode is simalar to the continuous mode with spread spectrum for load currents larger than $50\,mA$.

Output voltage using $Ro = 47\Omega$. The output voltage and its ripple at 31.9 mA are shown in Figures 2.19 and 2.20, respectivelly. The peak to peak ripple voltage is $5\,mV$, wich is larger than the one in continuous mode. In this operating mode the clock is turned off when the output

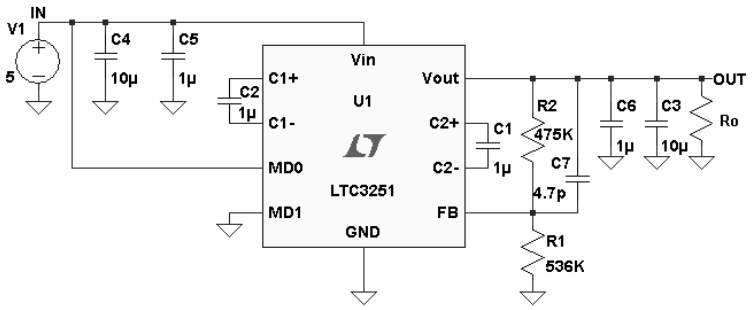

Figure 2.18: Schematic circuit used for the simulations in burst mode with spread spectrum.

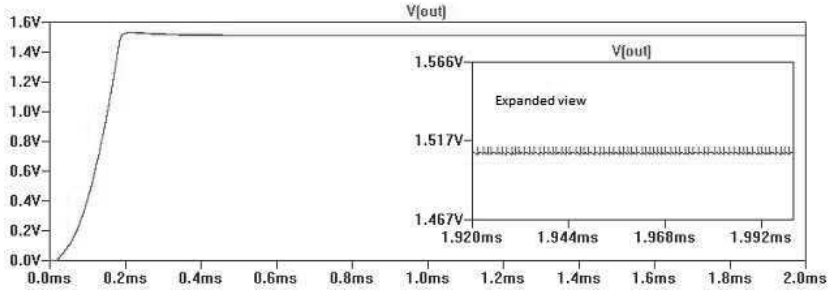

Figure 2.19: Output voltage at 31.9 mA.

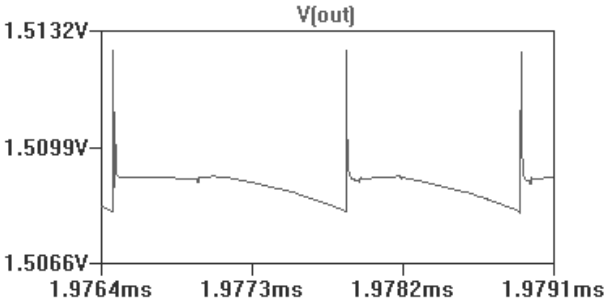

Figure 2.20: Output ripple voltage at 31.9 mA.

voltage reaches the upper threshold and turned back on when the voltage decreases and reaches the lower threshold. Turning off the clock oscillator increases the power efficiency.

Transient response to a load step. This simulation starts with an output current smaller then 50 mA (burst mode) that is later increased up to 500 mA (continuous mode). Figure 2.21 shows the load current and Figure 2.22 shows the corresponding output voltage. Notice the larger output ripple voltage in burst mode.

Line regulation. Figure 2.23 shows the line regulation for three different output currents.

Load regulation. Figure 2.24 shows the load regulation for Vin = 5 V.

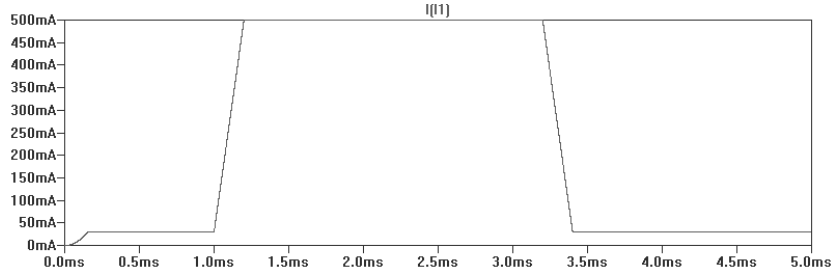

Figure 2.21: Load current transient.

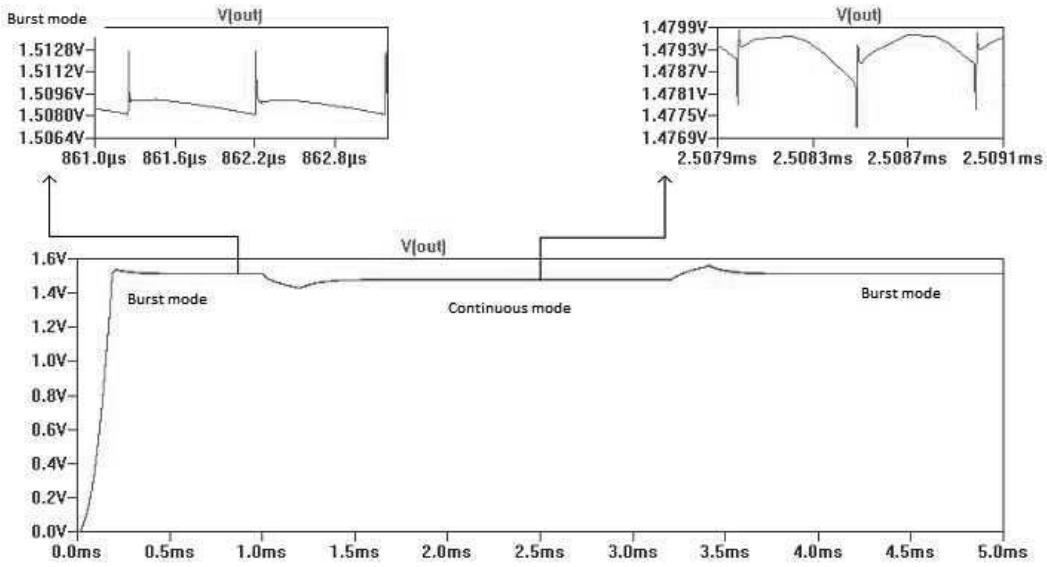

Figure 2.22: Output voltage transient response.

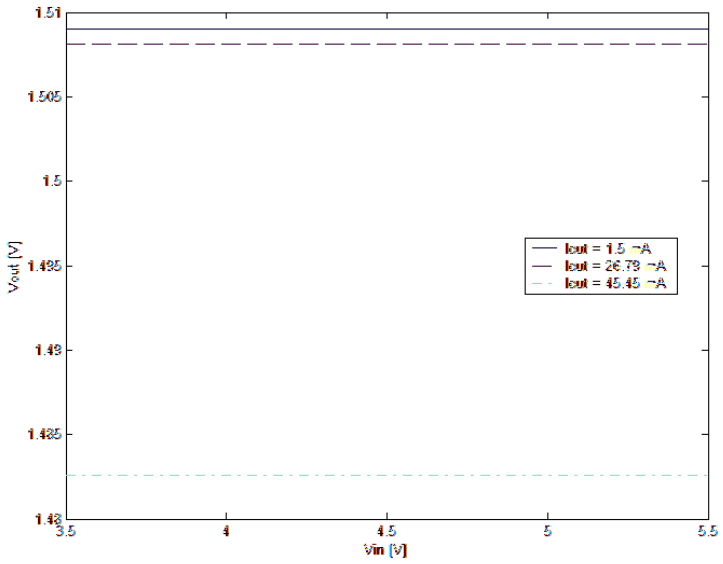

Figure 2.23: Line regulation for three different output currents in burst mode.

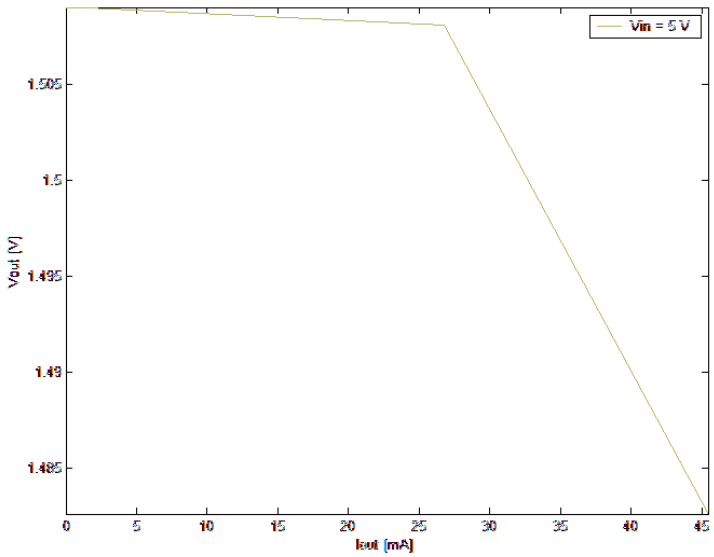

Figure 2.24: Load regulation in burst mode.

Super burst mode operation

The schematic circuit used for the simulations in super burst mode is shown in Figure 2.25.

Output voltage using Ro = 47Ω . Figure 2.26 shows the output voltage at 31.9 mA. The peak to peak amplitude is 30 mV for this operating mode. The ripple voltage is larger but the efficiency is improved.

Line regulation. Figure 2.27 shows the line regulation for two different load currents.

Load regulation. Figure 2.28 shows the load regulation in super burst mode for Vin = 5 V.

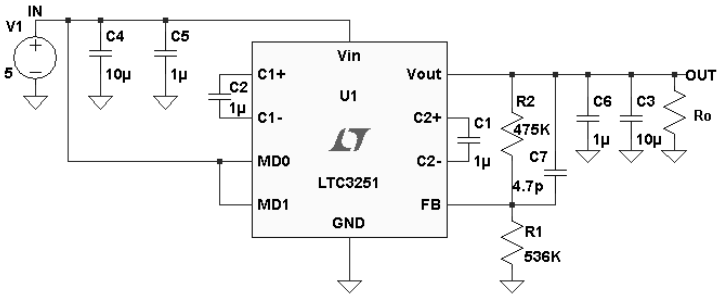

Figure 2.25: Schematic circuit used for the simulations in super burst mode.

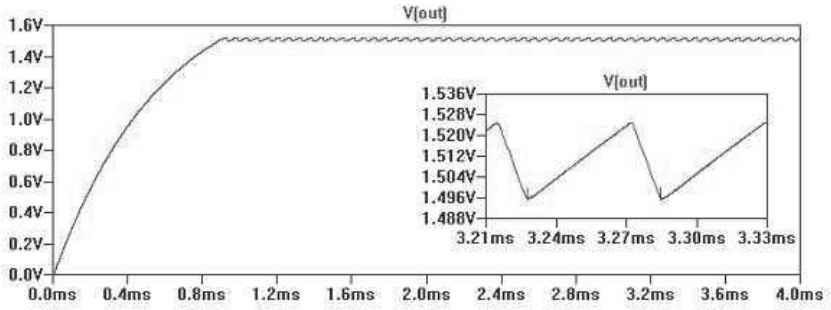

Figure 2.26: Output voltage at 31.9 mA.

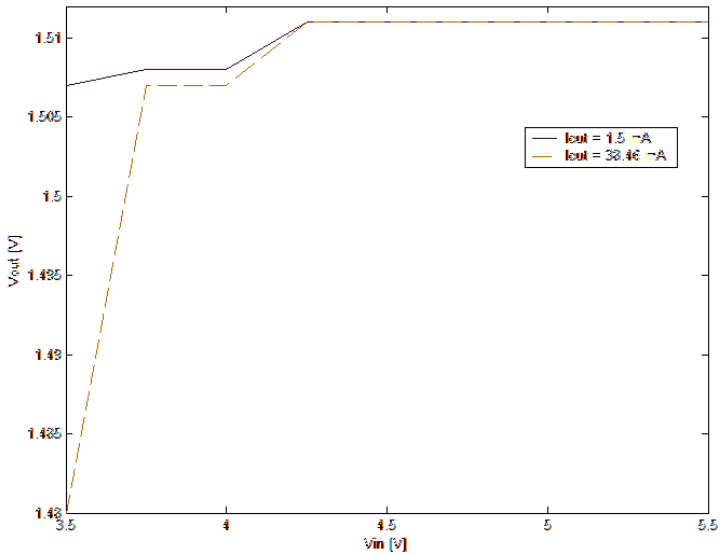

Figure 2.27: Line regulation for two different load currents in super burst mode.

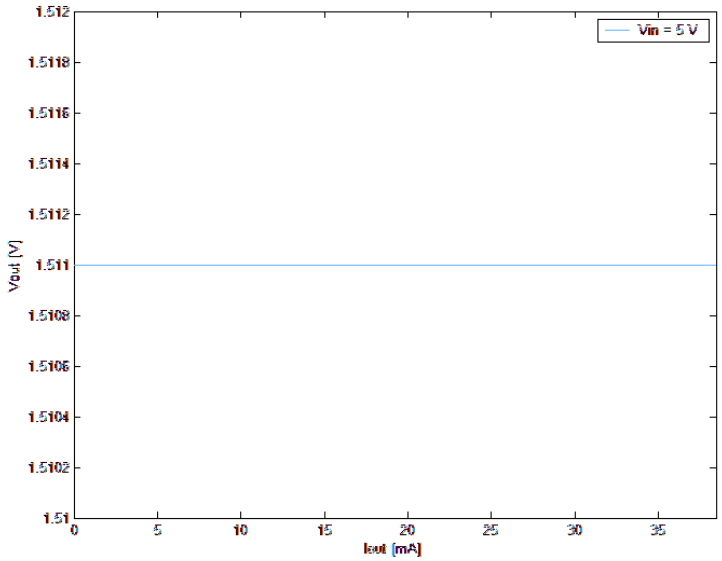

Figure 2.28: Load regulation for two different load currents in super burst mode.

Shortcircuit protection. Figure 2.29 shows the output current under shortcircuit operation. Notice that the current is limited to $800\,mA$.

Noise. Figure 2.30 shows the result of a Fourier analysis performed with a $45.45\,mA$ load. The frequency bins between $0.7\,MHz$ and $2\,MHz$ correspond to random frequency operation of the clock oscillator.

2.4. Experimental prototype

The schematic circuit of the experimental prototype is shown in Figure 2.31. The following differences are obvious from that of Figure 2.1 :

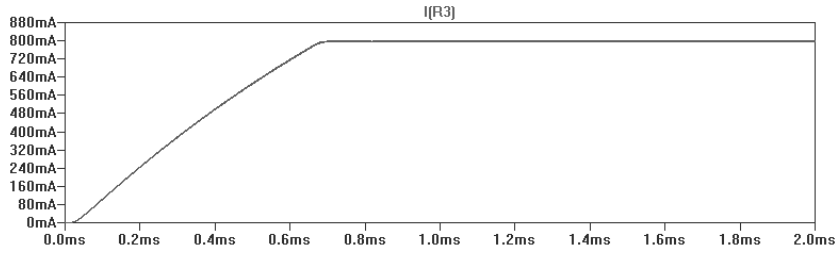

Figure 2.29: Output current under shortcircuit operation.

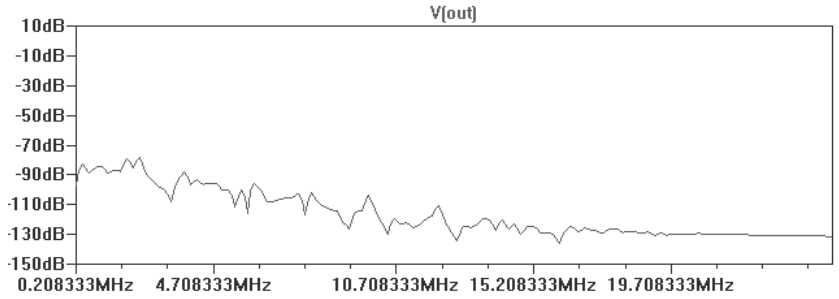

Figure 2.30: Fourier analysis.

- Power input connector E1, output power connector E3 and Mode connector E2.
- Jumpper Pu1 to disconnect the output filter from the LTC3251.
- Jumpers P1 and P2 to configure the operating mode.

Figure 2.32 shows the layout of the printed circuit board (scale: $1.8\,mm$ represent $1\,mm$). The top layer is in red, the bottom in blue. The tracks were kept as short as possible to reduce parasitic effects. Figure 2.33 shows a picture of the experimental prototype in actual scale.

Part List

Digi-Key Part Number	Manufacturer Part Number	Description	Manufacturer	Quantity
587-1300-1-ND	LMK212BJ106KG-T	CAP CER 10UF 10V X5R 0805	Taiyo Yuden	2
490-1702-1-ND	GRM219R61A105KC01D	CAP CER 1.0UF 10V 10% X5R 0805	Murata Electronics North America	4
478-1300-1-ND	08055A4R7CAT2A	CAP CERM 4.7PF 50V NP0 0805	AVX Corporation	1
311-536KCRCT-ND	RC0805FR-07536KL	RES 536K OHM 1/8W 1% 0805 SMD	Yageo	1
311-475KCRCT-ND	RC0805FR-07475KL	RES 475K OHM 1/8W 1% 0805 SMD	Yageo	1
311-10MARCT-ND	RC0805JR-0710ML	RES 10M OHM 1/8W 5% 0805 SMD	Yageo	2

2.5. Experimental results

Continuous mode with spread spectrum

Output voltage. Figures 2.34 and 2.35 show the output voltage waveforms at $1.5\,mA$ and $454.55\,mA$, respectively.

Line regulation. Figure 2.36 shows the line regulation in continuous mode for three different currents.

Load regulation. Figure 2.37 shows the load regulation in continuous mode for Vin$= 5\,V$.

Efficiency. Figure 2.38 shows the efficiency vs. the output current for Vin $= 5\,V$.

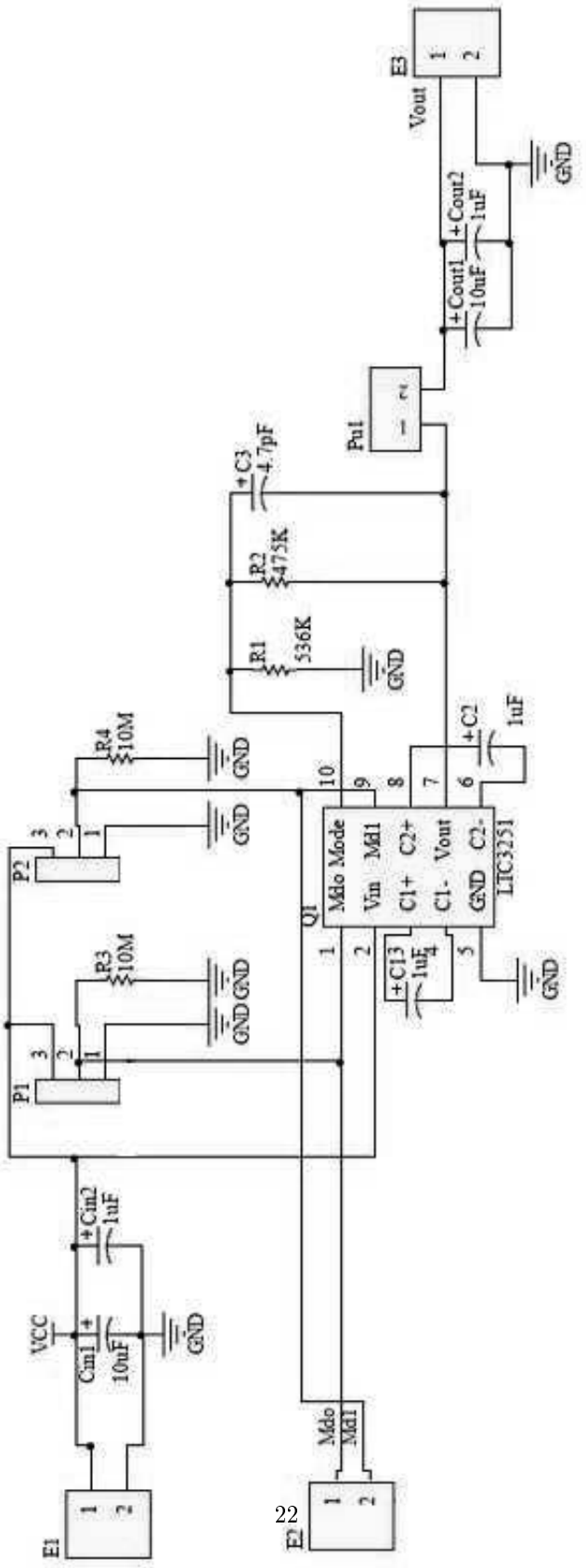

Figure 2.31: Schematic circuit of the experimental prototype.

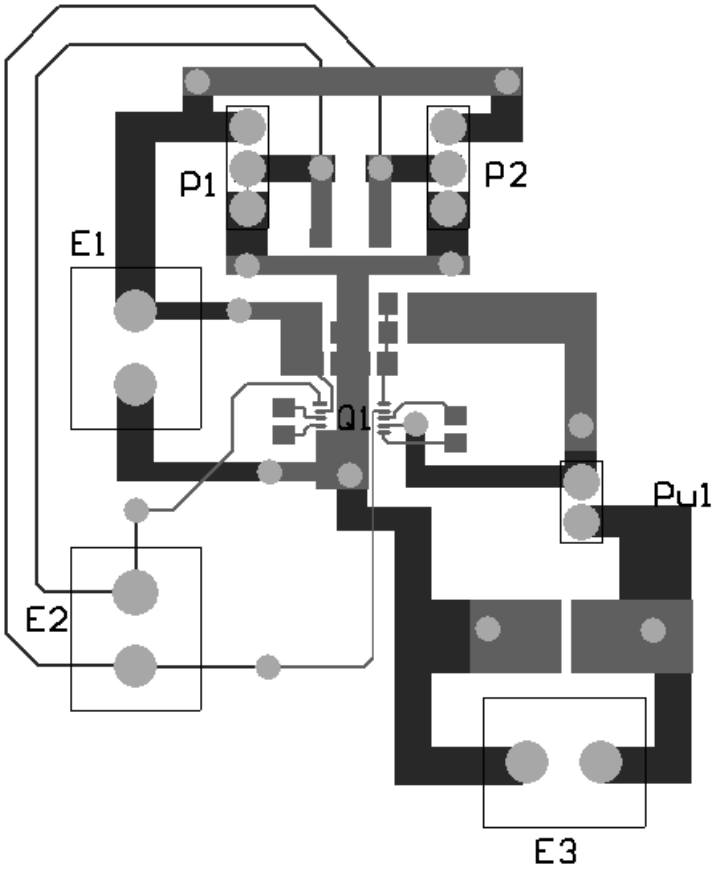

Figure 2.32: Layout of the printed circuit board.

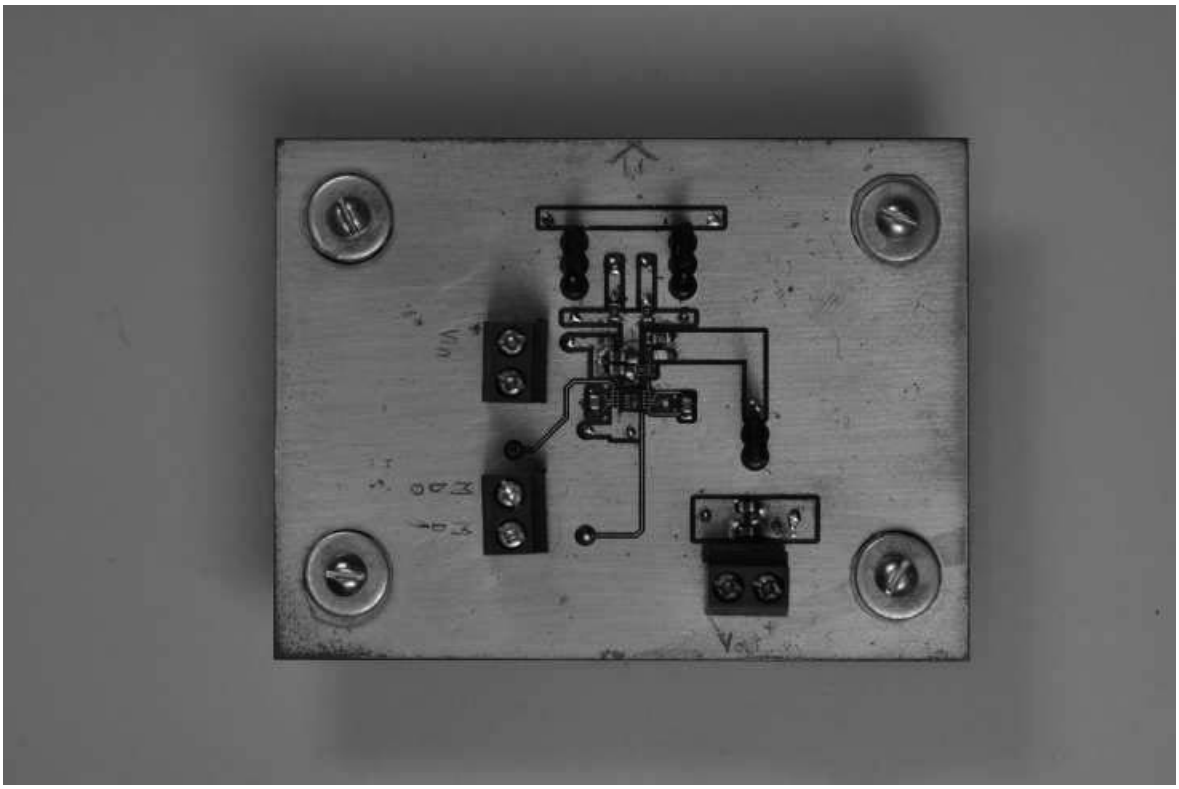

Figure 2.33: Picture of the printed circuit board.

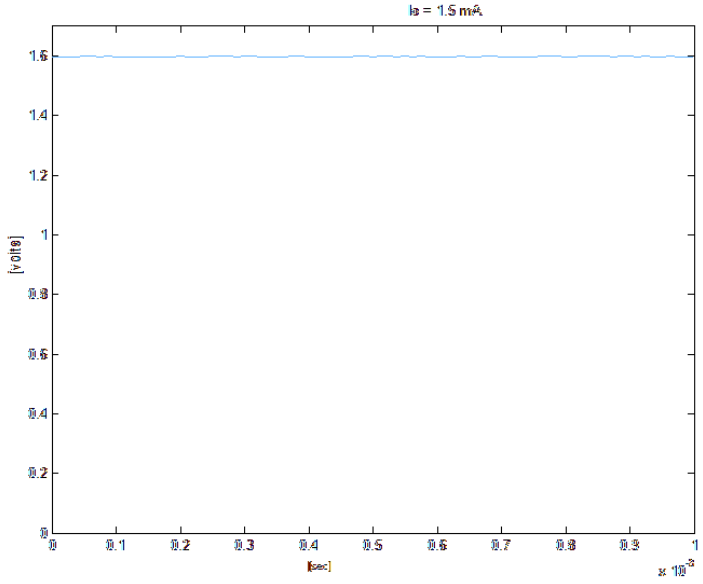

Figure 2.34: Output voltage waveforms at 1.5 mA.

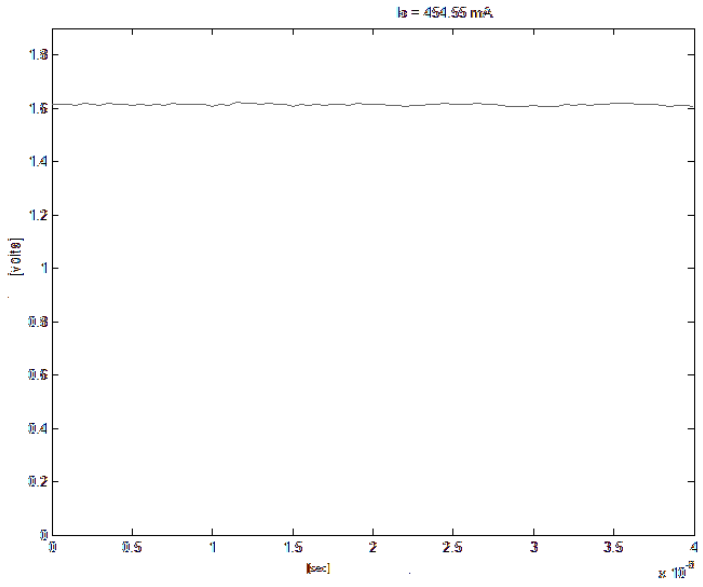

Figure 2.35: Output voltage waveforms at 454.55 mA.

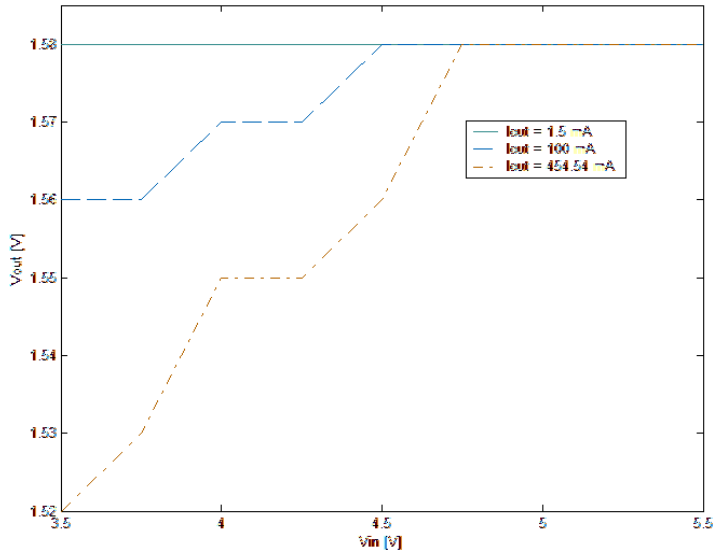

Figure 2.36: Line regulation in continuous mode.

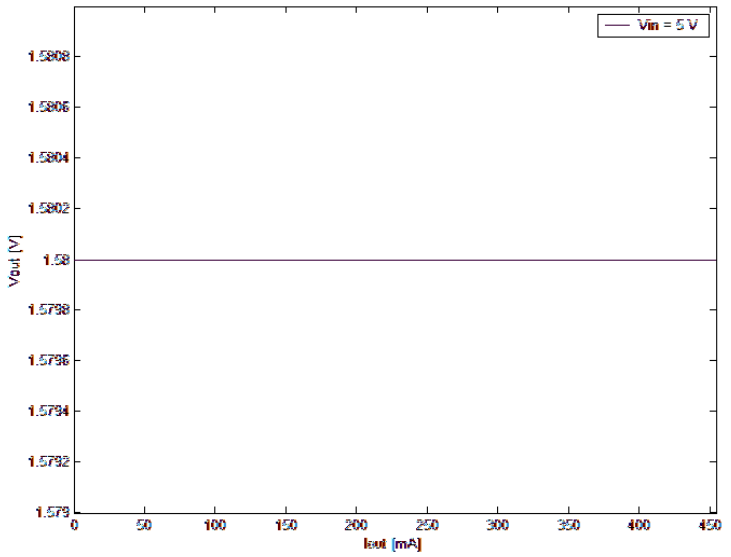

Figure 2.37: Load regulation in continuous mode.

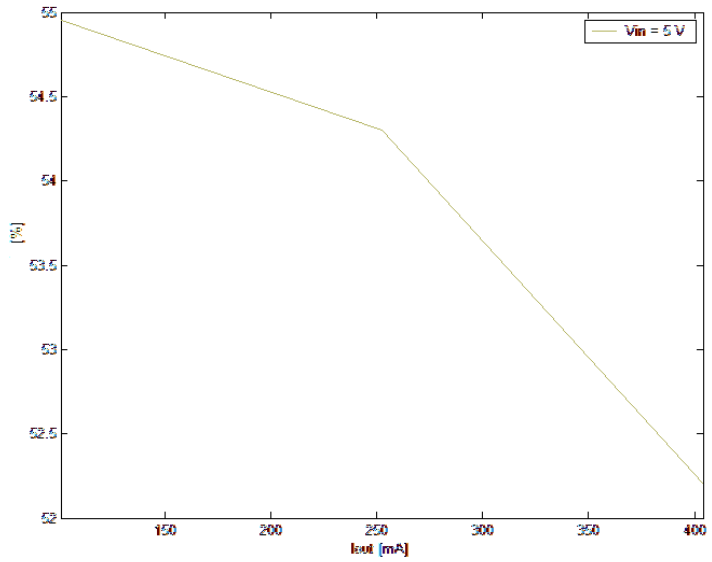

Figure 2.38: Efficiency vs. the output current in continuous mode.

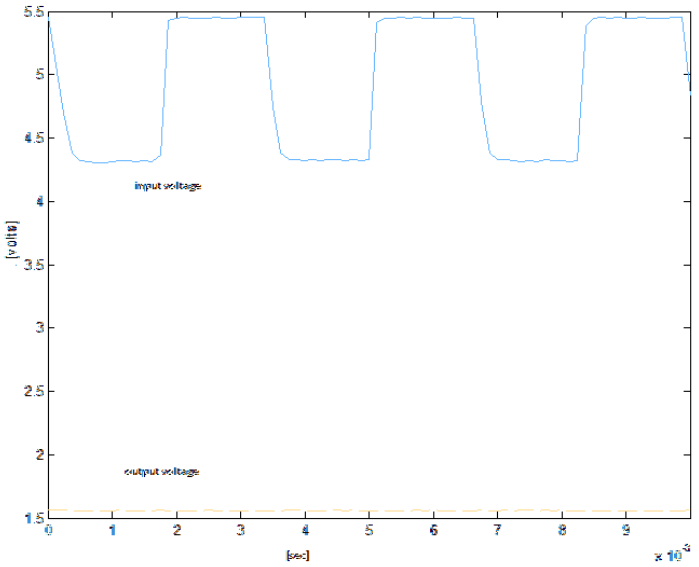

Figure 2.39: Input and output voltages in continuous mode.

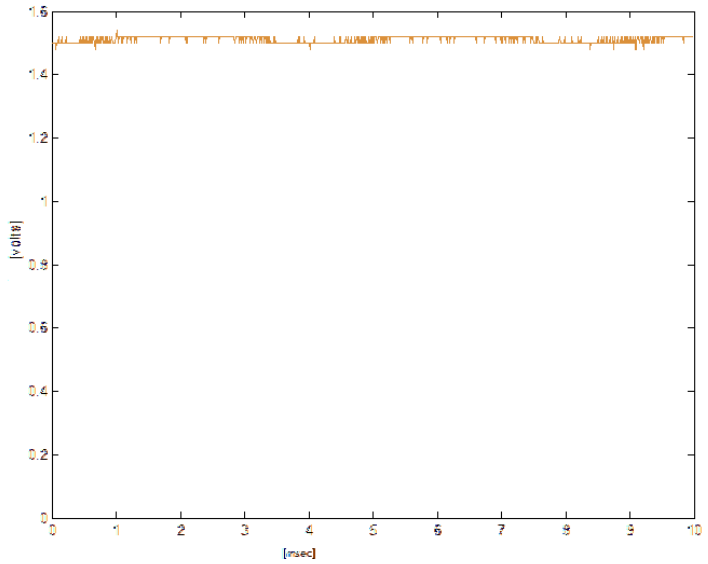

Figure 2.40: Output voltage with varing load.

Input voltage transient. A $300\,Hz$ square waveform was injected in series with the DC input voltage. The input voltage changed from $4.31\,V$ to $5.44\,V$. The input and output voltages are shown in Figure 2.39 for an output current of $252.31\,mA$.

Transient response for a load change. An active load was set with the following parameters:

- minimum current: $50\,mA$;
- maximum current: $475\,mA$;
- frequency: $200\,Hz$;
- duty cycle (D): $40\,\%$.

Figure 2.40 shows the output voltage whith the active load.

Burst operating mode with spread spectrum

Output voltage. Figure 2.41 shows the output voltage at $31.9\,mA$.

Line regulation. Figure 2.42 shows the line regulation fot three different loads.

Load regulation. Figure 2.43 shows the load regulation in burst mode for Vin $= 5\,V$.

Efficiency. Figure 2.44 shows the efficiency vs. the output current when the input voltage is $5\,V$.

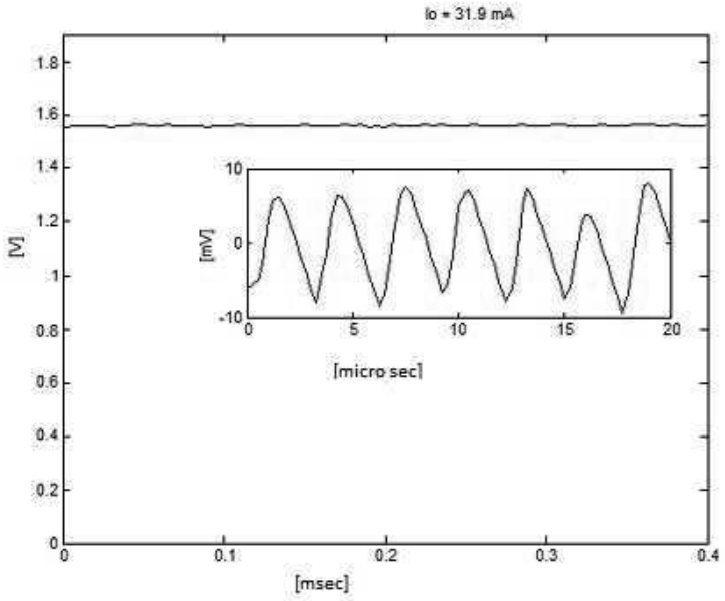

Figure 2.41: Output voltage in burst mode.

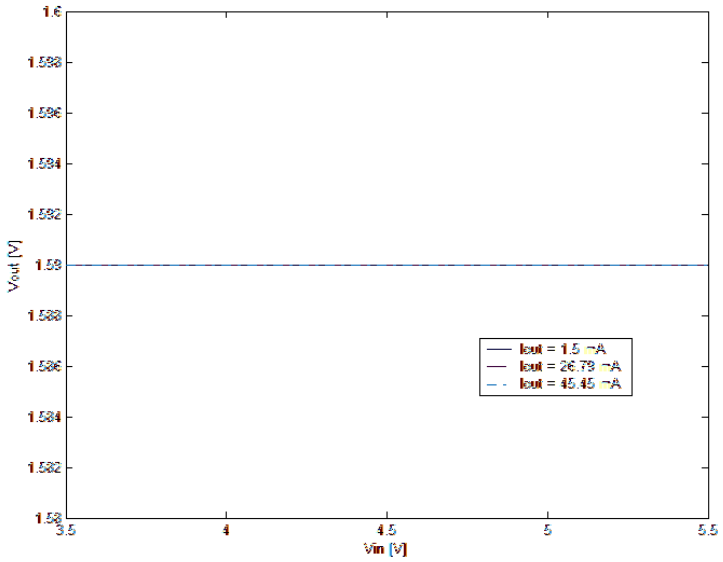

Figure 2.42: Line regulation in burst mode.

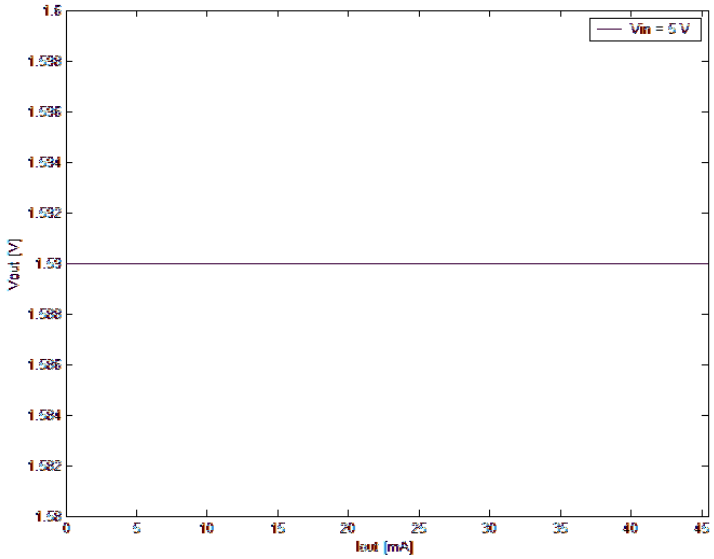

Figure 2.43: Load regulation in burst mode.

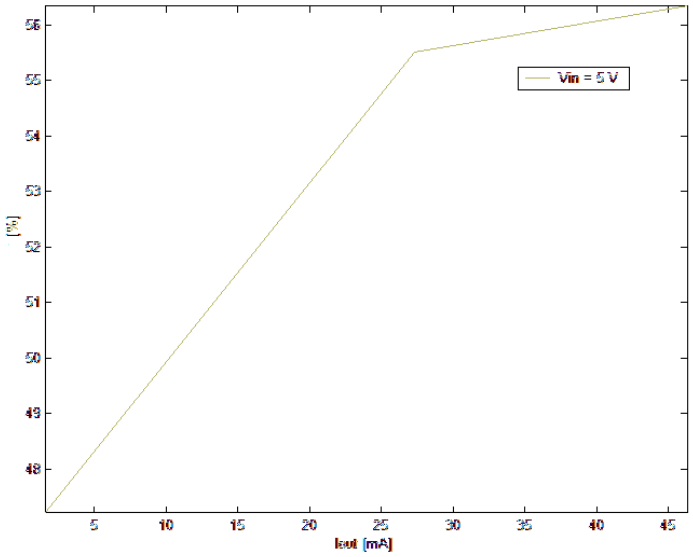

Figure 2.44: Efficiency vs. the output current in burst mode.

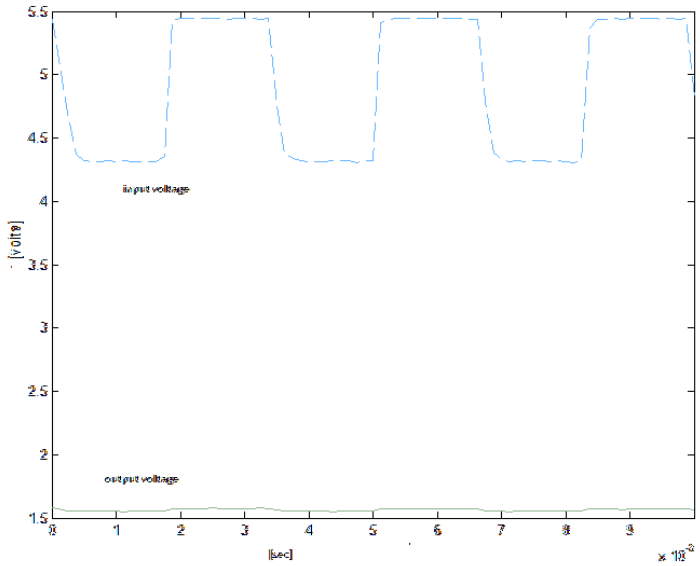

Figure 2.45: Input and output voltages in burst mode.

Input voltage transient. The input voltage was veried from $4.25\,V$ to $5.44\,V$ at $300\,Hz$. The input and output voltage waveforms are shown in Figure 2.45 for a load of $252.31\,mA$.

Output current transient. The active load was set to:

- minimum current $30\,mA$;
- maximum current $475\,mA$;
- frequency $200\,Hz$;
- duty cycle (D): $40\,\%$.

Figure 2.46 shows the output voltage waveform when the active load was connected.

Super burst mode with spread spectrum

Output voltage. Figure 2.47 shows the output voltage waveform at $31.9\,mA$.

Line regulation. Figure 2.48 shows the line regulation in super burst mode for two different loads.

Load regulation. Figure 2.49 shows the load regulation for Vin $= 5\,V$.

Efficiency. Figure 2.50 shows the efficiency vs. the output current for Vin $= 5\,V$.

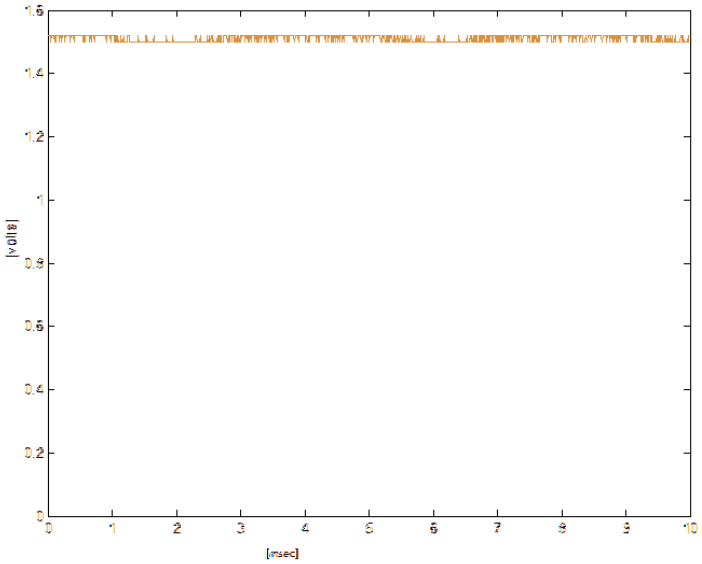

Figure 2.46: Output voltage with varying load.

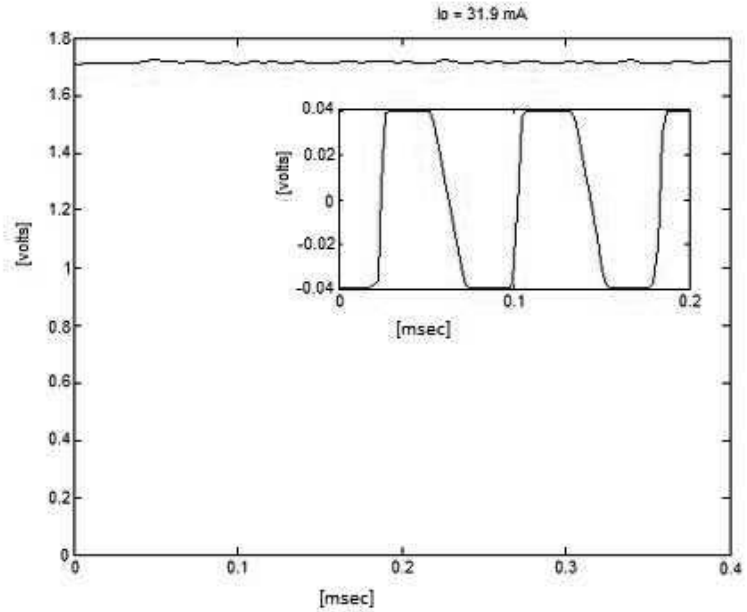

Figure 2.47: Output voltage waveform in super burst mode.

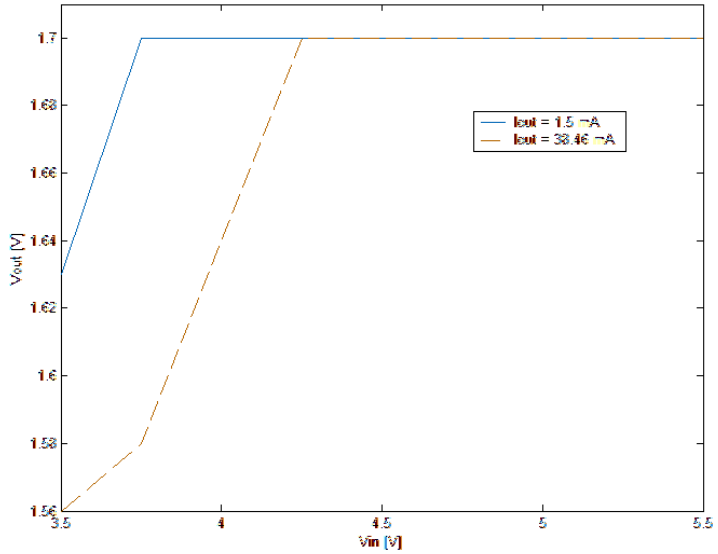

Figure 2.48: Line regulation in super burst mode.

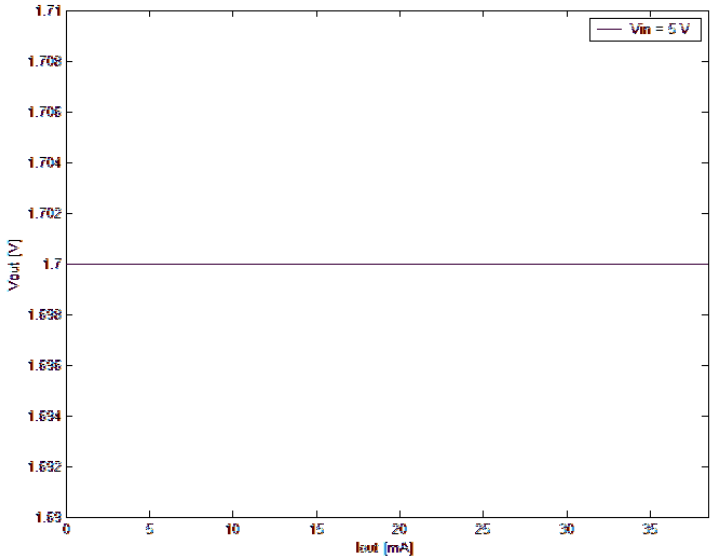

Figure 2.49: Load regulation in super burst mode.

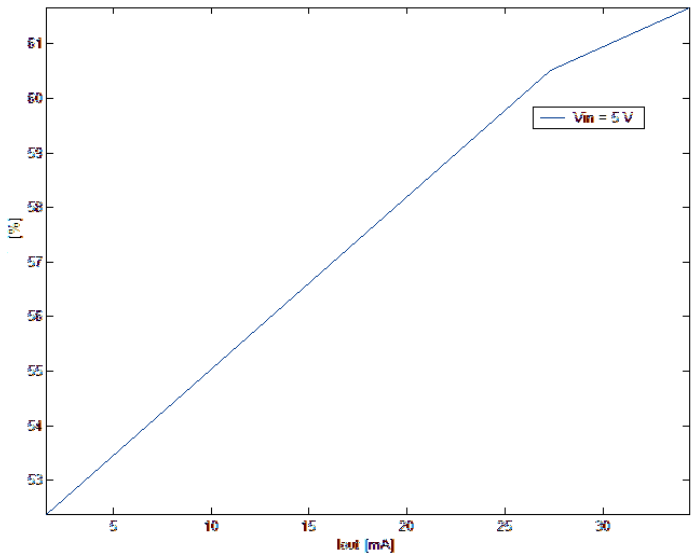

Figure 2.50: Efficiency vs. the output current in super burst mode.

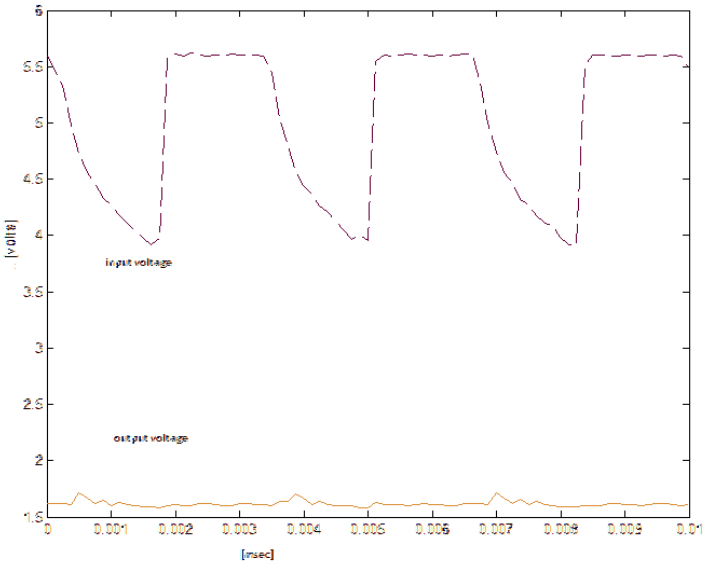

Figure 2.51: Input and output voltage waveforms in super burst mode.

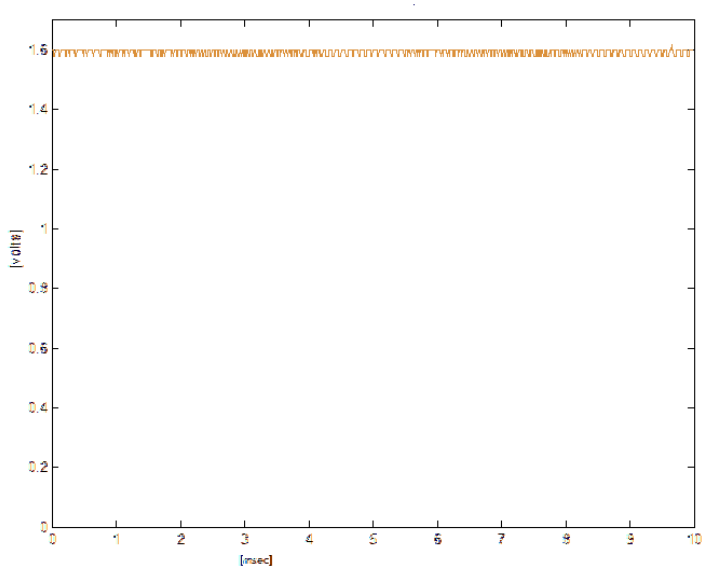

Figure 2.52: Output voltage waveform due to a load transient.

Input voltage transient. The input voltage source was varied from $3.88\,V$ to $5.63\,V$ at a rate of $300\,Hz$. The input and output voltage waveforms are shown in Figure 2.51 for a load current equal to $34.368\,mA$.

Load transient. The active load was set with the following parameters:

- minimum current $5\,mA$;
- maximum current $35\,mA$;
- frequency $200\,Hz$;
- duty cycle (D): $40\,\%$.

Figure 2.52 shows the corresponding output voltage waveform.

2.6. Conclusion

The switching converter performed as expected. Simulation and experimental results show a good match.

EMI compliance was not tested.

The power efficiency is acceptable for all load levels. Noitice that it is lower than the efficiency expected from a conventional switching converter, but larger than the efficiency of an equivalent linear voltage regulator.

Table 3: Design specifications.

Parameter	Minimum	Typical	Maximum	Unit
Vin	3.5	5	6	V
Vout	11.76	12	12.24	V
Iout			500	mA
output voltage ripple			10	mV_{pp}
Fosc	74.42	100	124	kHz

3. Low-noise step-up DC-DC converter

- Design a low-noise step-up DC-DC converter based in the LT1738 integrated circuit using the circuit topology shown in Figure 3.1, with the specifications summarized in Table 1. Compare the component values obtained in your design with those given in Figure 2.1. The student should read first the data sheets of the LT1738 IC before proceeding.
- Run simulations using LTSPICE to verify the design.

  Output voltage using Ro = $120\,\Omega$

  Output voltage using Ro = $24\,\Omega$

  Verify the rise and fall time control

  Transient response to a load step

  Line regulation

  Load regulation

  Noise
- Build a prototype using the provided gerber file and part list.
- Obtain the following experimental results

  Output voltage for a load current equal to $12\,mA$, $100\,mA$ and $500\,mA$

  Transient response to a load step

  Transient response to an input transient

  Line regulation

  Load regulation

  Noise

  Efficiency

3.1. LT1738

Figure 3.2 shows the pin assignment of the LT1738. Refer to the data sheet for a description of each pin functionality.