Chapter 2

Sampling and Reconstruction

Problem Solutions

1. In theory, the highest frequency that can be sampled in lowpass sampling (as opposed to bandpass sampling) without aliasing is $0.5F_s$. Thus, in this example, 24 kHz would be the highest frequency that could be sampled without aliasing. Note that real-world constraints, such as non-ideal reconstruction filters, would reduce this by at least 10%.

2. Since 30 kHz is 6 kHz above the "wrap-around" frequency of 24 kHz, the resulting aliased signal would appear at $24 - 6 = 18$ kHz.

3. For a dynamic range D and b-bit samples, the approximate resolution (or LSB voltage) is

$$\frac{D}{2^b} = \frac{2 \text{ V}}{2^{16}} = 30.52 \ \mu\text{V}$$

4. In general, the SQNR (in decibels) is estimated by:

$$\text{SQNR}_{\text{dB}} = 10 \log_{10} \frac{\sigma_x^2}{\sigma_e^2}$$

where σ_x^2 is the input signal variance representing the signal power and σ_e^2 is the quantization noise variance representing quantization noise power. For an ADC with dynamic range D and b-bit samples, and using common assumptions about the quantization error, this becomes

$$\text{SQNR}_{\text{dB}} = 10 \log_{10} \left(\frac{2^{2b} \cdot 12 \cdot \sigma_x^2}{D^2} \right) = 6.02b + 10.79 - 20 \log_{10} \left(\frac{D}{\sigma_x} \right).$$

This shows the well known relation that SQNR increases by approximately 6 dB for each 1-bit increase in the number of bits per sample. To calculate the third term of the equation above, an assumption must be made regarding the input signal type, since this term depends upon the standard deviation σ_x (which is equivalent to the RMS value). If we assume a sinusoid with an amplitude of A, the RMS value is $A/\sqrt{2} = 0.7071A$. According to the problem, the signal has an amplitude of $A = 1$ V, and the dynamic range of the ADC is $D = 2$ V, and the number of bits is 16. Thus, for the sinusoidal assumption,

$$\text{SQNR}_{\text{dB}} = (6.02)(16) + 10.79 - 20 \log_{10} \left(\frac{2}{0.7071} \right) = 98.08 \text{ dB}.$$

Noise shaping methods, such as those commonly employed in sigma-delta ADCs, can produce a higher SQNR than this.

5. A unit-amplitude sinusoidal signal of frequency f_0 that is sampled at a sample frequency F_s, such that $f_0 = 0.5F_s$, will produce samples having the pattern $+1, -1, +1. -1, \ldots$ (assuming the phase

relationship between the signal and the sample clock are optimal). Point-by-point multiplication of this pattern by an arbitrary input signal is equivalent to changing the sign of every other sample of the arbitrary input signal. Since multiplication in the time domain results in modulation, it follows that changing the sign of every other sample of an input signal is equivalent to modulating the input signal by a sinusoid with a frequency of one-half the sample frequency (i.e., $0.5F_s$).